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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Application of: Art Unit: 2503

Vora Examiner: S. CRANE

Serial No. 08/654,760

Docket No. V&F-001.CPA1

Filed: 5/29/96

For: VERTICALLY INTEGRATED FLASH EEPROM FOR GREATER DENSITY AND LOWER COST

30/F
FJONES
1-6-03

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Morgan Hill, California
December 16, 2002

SUPPLEMENTARY AMENDMENT

Dear Sir:

In further response to the Office Action mailed 8/1/2002 and in light of the comments of the Examiner at the interview, please amend the above identified case as follows and consider the following new evidence.

IN THE CLAIMS

1. (Clean) A nonvolatile EPROM or EEPROM memory cell formed using a vertical MOS transistor comprising:

a semiconductor substrate doped to have a first conductivity type so as to act as a source region of said nonvolatile memory cell, said first conductivity type being either N-type or P-type, and having a top surface which extends laterally and a depth which extends vertically;

a vertical MOS transistor formed by alternating, abutting N-type and P-type doped layers in said substrate which have junctions therebetween to form a channel region and a